**Tutorial Problems on Counters and Shift Registers**

1. Design a mod-12 synchronous counter using T FFs.
2. Design a J-K counter that goes through states 2, 4, 5, 7, 2, 4, …Modify the circuit such that whenever it goes to any invalid state it comes back to state 7.
3. Design a counter with T FFs so that it must go through the states 0, 2, 5, 7, 3, 0, … if the control line is HIGH and through states 0, 4, 2, 6, 1, 0, …if the control line is LOW.
4. Design a shift register pulse train generator to generate the pulse train 11110010
5. Design an up/down counter using D FFS to count 0, 3, 2, 6, 4, 0, ….
6. Design a 3-bit synchronous up/down counter.
7. Design and implement a mod-10 asynchronous counter using T FFs.
8. Design a synchronous sequential circuit which produces an output z = 1, whenever any one of the following input sequences 1100, 1010, or 1001 occurs. The circuit resets to its initial state after a 1 output has been generated.
9. Design and implement a 4-bit parallel-in, serial-out shift register using D FFs. There must be two control lines (i) for loading and shifting and (ii) for resit.
10. Design a 5-bit Linear Feedback Shift Register (LFSR) that generated 31-distinct pseudo random patterns (excluding all zero state) in sequence. Draw the diagram.